atoms from the BPSG insulating layer 24 migrate into the adjacent source/drain regions 40 and under the nitride spacers 32 in the LDD regions 42 during these high-temperature steps. Although the boron/phosphorous migration into the source/drain regions 40 occurs in limited regions, near or at a source/drain -BPSG interface 51 (Figure 2), this interface is degraded and the performance of the device affected. A major drawback posed by the migration of impurity boron/phosphorous atoms at the source/drain-BPSG interface 51 is the decrease in the "refresh time" of the DRAM device, and consequently an increase in the DRAM error rate. The "refresh time" of a DRAM cell is defined as the length of time over which the DRAM cell can retain a sufficient amount of charge for its intended data state to be determined by a sense amplifier circuit. Before this period of time expires, the DRAM cell must be reprogrammed or "refreshed" and, consequently, it is desirable that the refresh time between the refresh operations be as long as possible.

A1 Cont.

Current Claims:

1. A method of forming a composite insulating structure, comprising:

forming at least one gate stack structure over a substrate;

forming a source/drain region in said substrate on opposite sides of said gate stack structure;

NE

forming an oxide layer over at least said source/drain region, said oxide layer being formed by oxidizing an upper surface of said source/drain region using atomic oxygen; and

forming a barrier layer over said oxide layer.